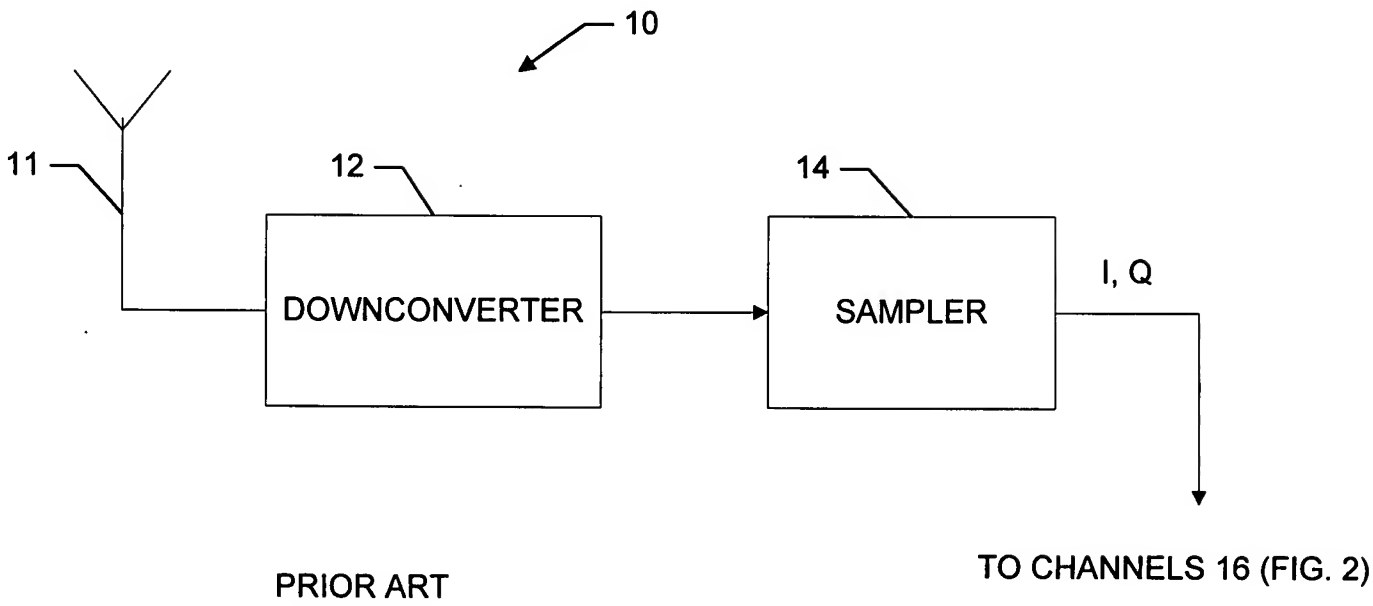
10
11
12
14
DOWNCONVERTER
SAMPLER
I, Q
PRIOR ART
TO CHANNELS 16 (FIG. 2)

FIG. 1

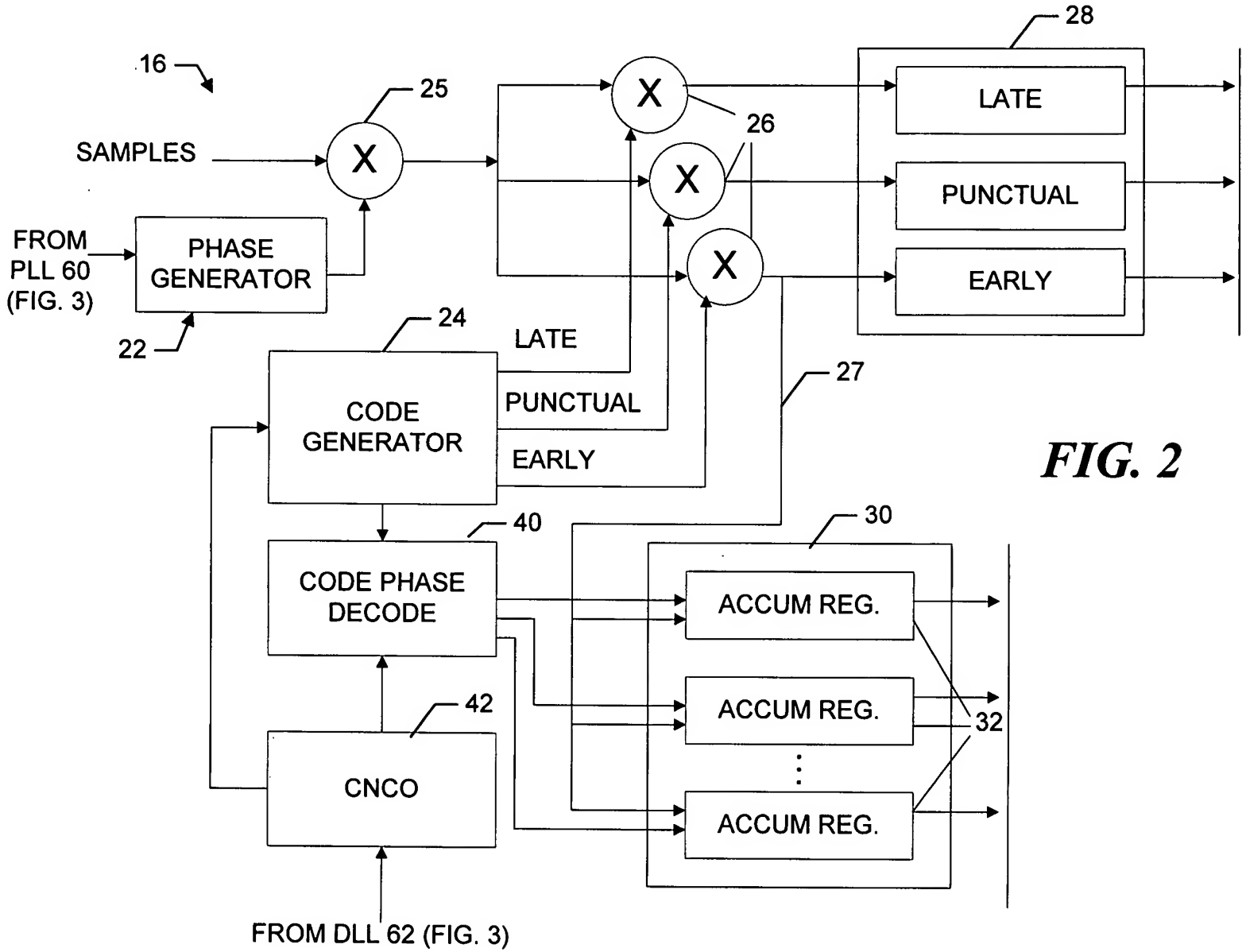
16
25
SAMPLES
X
X
X
X
26
28
LATE
PUNCTUAL
EARLY
FROM
PLL 60
(FIG. 3)
PHASE
GENERATOR
22
24
LATE
CODE
GENERATOR
PUNCTUAL
EARLY
27
40
CODE PHASE
DECODE
30
ACCUM REG.
ACCUM REG.
ACCUM REG.
32
42
CNCO
FROM DLL 62 (FIG. 3)

FIG. 2

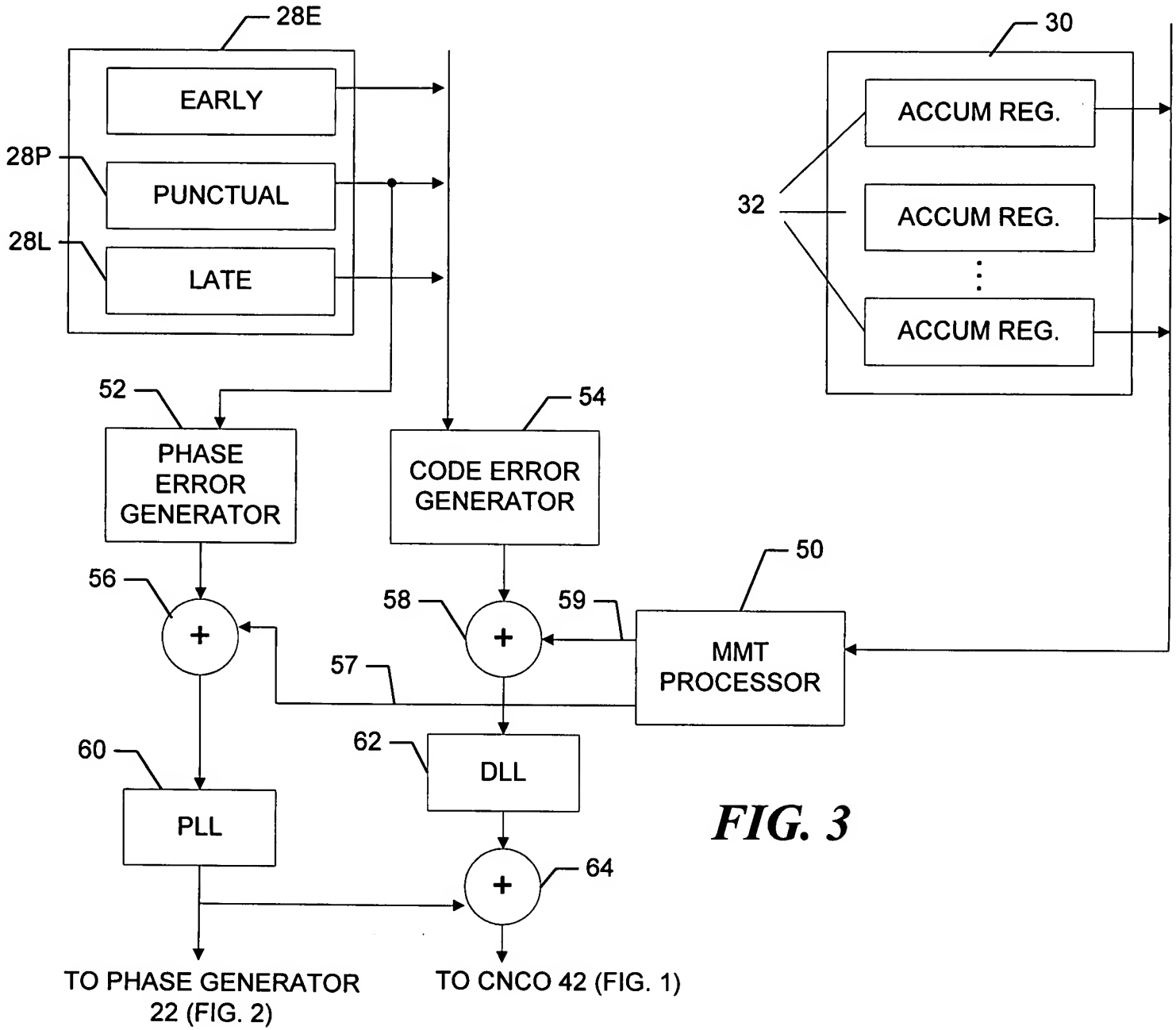
28E
EARLY
28P
PUNCTUAL
28L
LATE
30
32
ACCUM REG.
ACCUM REG.
ACCUM REG.
52
PHASE ERROR GENERATOR
54
CODE ERROR GENERATOR
50
56
58
59
57
MMT PROCESSOR
60
PLL
62
DLL
64
TO PHASE GENERATOR 22 (FIG. 2)
TO CNCO 42 (FIG. 1)

FIG. 3

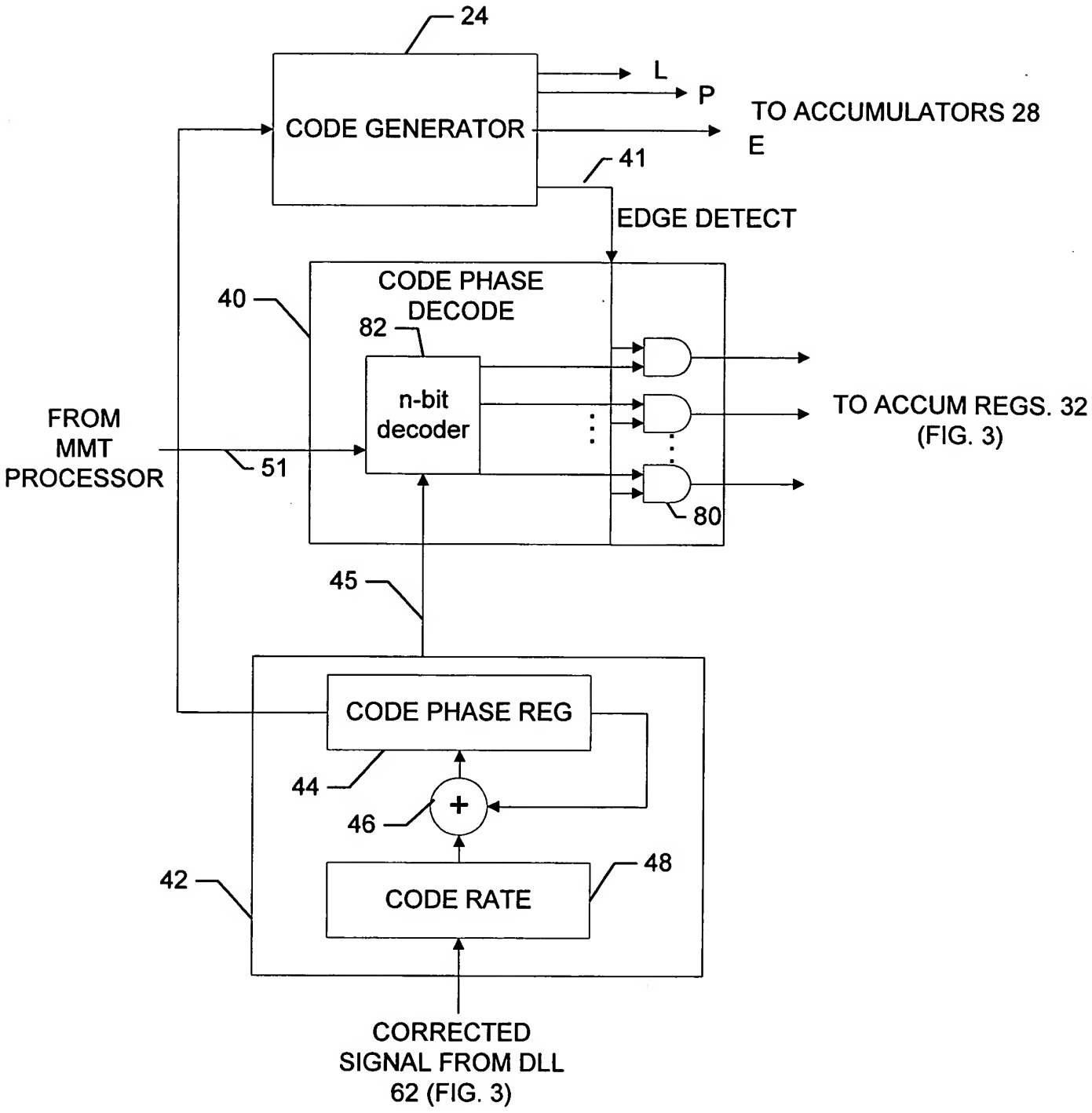
24
CODE GENERATOR
L
P
E
TO ACCUMULATORS 28
41
EDGE DETECT
CODE PHASE
DECODE
40
82
n-bit
decoder
TO ACCUM REGS. 32
(FIG. 3)
FROM
MMT
PROCESSOR
51
80
45
CODE PHASE REG
44
46
42
48
CODE RATE
CORRECTED
SIGNAL FROM DLL
62 (FIG. 3)

FIG. 4

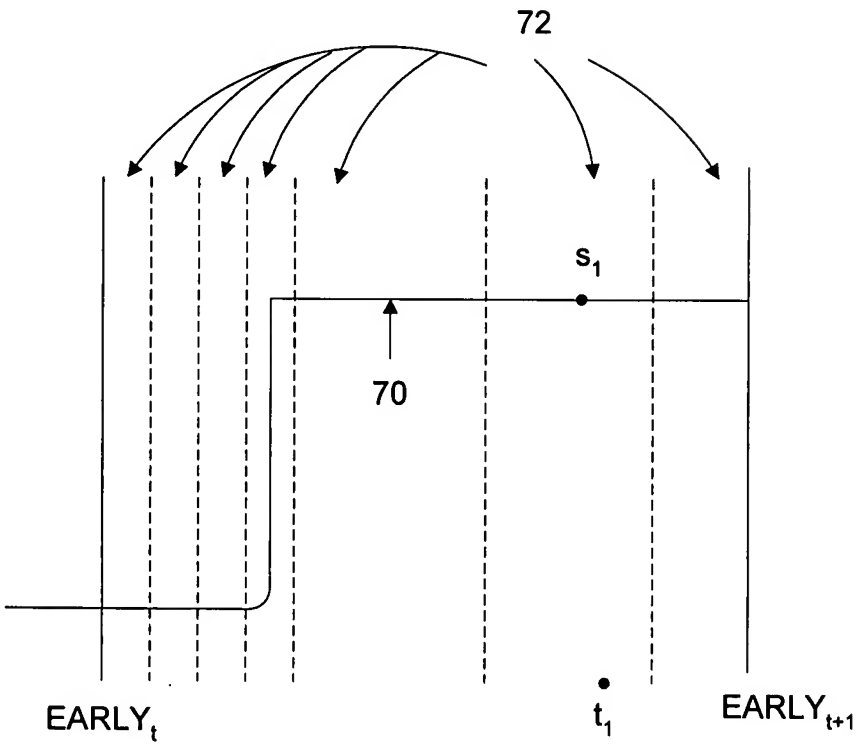

FIG. 5

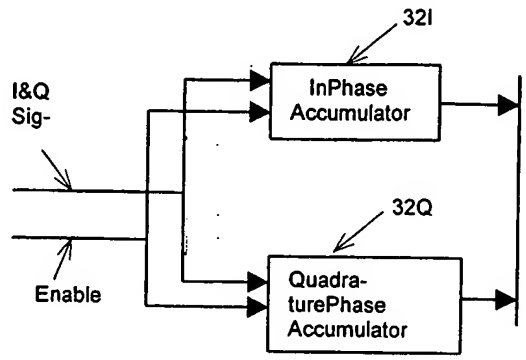
32I
InPhase
Accumulator
I&Q
Sig-
32Q
Enable
Quadra-
turePhase
Accumulator

Fig 6

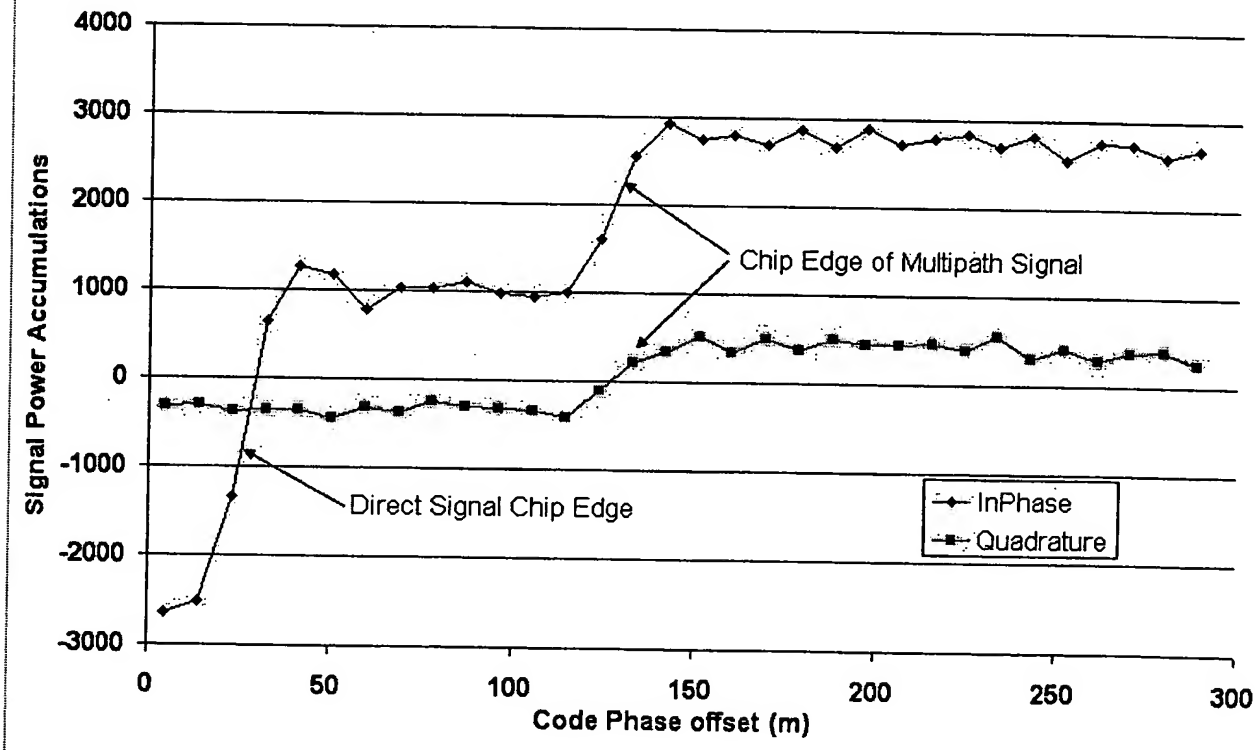
4000
3000
2000
1000
0
-1000
-2000
-3000
Signal Power Accumulations
0
50
100
150
200
250
300
Code Phase offset (m)
Chip Edge of Multipath Signal
Direct Signal Chip Edge
InPhase
Quadrature

Fig 7